REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-23 and 27-29 are presently active in this application, Claims 1, 8, 15, 21, 22, 23, 27 and 28 having been amended and new Claim 29 added by the present Amendment.

In the outstanding Office Action Claims 1-23 were rejected under 35 USC §102(e) as being anticipated by Dutton et al (U.S. Patent 6,061,756, hereinafter "Dutton").

First, Applicants respectfully point out that the outstanding Official Action did not address the merits of Claims 27-28 added by the amendment filed Sept. 27, 2004. Applicants therefore respectfully request formal consideration on the merits in response to filing of the present amendment. Entry and consideration of this amendment on that basis is respectfully requested.

By way of this amendment and reply to the Office Action mailed January 5, 2005, Claims 1, 8, 15, 21-23, and 27-28 have been amended; and Claim 29 has been newly added. Support for the amendments to independent claims 1, 8, 15 and 21 - 23 may be found on page 8, lines 6 to 13 of the specification and Fig. 5 of the drawings. Support for the amendments to dependent claims 27 and 28 may be found in Fig. 6. Support for the amendments to newly added independent claim 29 may be found at page 9, lines 7 to 33 of the specification and Figs. 5 and 6 of the drawings. Therefore, no new matter has been added.

Applicants respectfully traverse the rejection of Claims 1-23 under 35 U.S.C. 102(e), as being anticipated by Dutton, because in Applicants' view, the claimed invention is clearly patentably distinguishing over the cited art.

In particular, with regard, to Claims 1, 8 and 15, 21-23, the outstanding Official Action states that Dutton discloses a data transfer control circuit for carrying out data transfer

by using a plurality of bus masters, including a data bus (130) connected to a peripheral

apparatus (142-146), said data bus having of a plurality of unit data buses (channels) each of

which transfers data concurrently (col. 5, lines 24-34); a plurality of bus masters configured

to send a request signal requesting a use of said data bus in unit data buses, and to use said

data bus in unit data buses requested when a request by means of said request signal is

granted (col. 9, lines 19-25) ; and a bus controller (222) configured to split-control said data

bus in unit data buses for said plurality of bus masters by giving a grant signal which grants

the use of said data bus in unit data buses requested in unit data buses to said bus masters in

accordance with an availability of said data bus in unit data buses (col.10, lines 26-58),

wherein the request signal has a data field comprising a plurality of bits, each of said plurality

of bits corresponding to a respective one of said unit data buses (col. 10, lines 26-39), and

said bus controller grants the use of each of said unit data buses specified by the bits of said

request signal (col. 9, line 40-col. 10, line 67).

However, with regard to the amended independent claims 1, 8 and 15, 21-23, there is

provided:

A data transfer control circuit, comprising:

a data bus connected to a peripheral apparatus, said data bus having a

plurality of unit data buses, each of which transfers data concurrently;

a plurality of bus masters <u>connected to each of the unit data buses and</u>

configured to send a request signal requesting a use of each of said unit data

buses, and to use said unit data buses requested when a request by means of

said request signal is granted; and

one bus controller <u>connected to all of the bus masters and</u> configured to

split-control said unit data buses for said plurality of bus masters by giving a

grant signal <u>to the bus masters,</u> which grants the use of each of said unit data

buses in accordance with said request signal, wherein

the request signal has a field comprising a plurality of bits, each of said

plurality of bits corresponding to a respective one of said unit data buses, and

said bus controller grants the use of each of said unit data buses specified by

the bits of said request signal.

As apparent from the claimed recitation of a <u>one</u> bus controller connected to all of the

bus masters (such as CPUs and DMACs), the claimed invention enables centralized-control

of a plurality of bus masters in bus arbitration.

In contrast, <u>Dutton</u> only discloses the method for <u>non-centralized</u> arbitration for use of

a byte sliced bus 120 in a computer system (col., 10, lines 13-19). In particular, in <u>Dutton</u>,

there is provided a plurality of arbitration logics 222A,B, which the outstanding Official

Action identifies with the claimed bus controller, and the arbitration logics 222A,B are

incorporated into each of multimedia devices 142, 144, 146, which the outstanding Official

Action identifies with the claimed bus masters, (col., 10, line 25, Figs. 2-4), while the claimed

bus controller is provided outside of bus masters and connected to all of the bus masters to

centrally control all bus masters. In <u>Dutton</u>, since no supervisor is provided unlike in the

claimed invention, each data packing logic 178 and byte slicing logic 176 in each of the

respective devices 142-146 have to monitor traffic on the plurality of data channels to

determine availability of each of the plurality of data channels, for permitting each arbitration

logic 222 in the respective device 142-146 to assert ownership of the available one or more

data channels (col., 10, lines 29-49). As no information is notified to each arbitration logic

222 in the respective device 142-146 whether the other device 142-146 is to request

ownership of the data channels, the arbitration method in <u>Dutton</u> raises many collisions

between the sending device and another sending device (col., 10, lines 53-58). Consequently,

<u>Dutton</u> completely fails to disclose claimed one bus controller connected to all of the bus

masters, as claimed. Accordingly, it is respectfully submitted that the outstanding rejection on the merits is traversed.
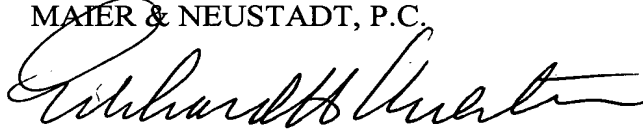
Turning now to dependent Claims 27 and 28, which were added in the previous amendment but not treated in any respect in the outstanding Official Action, Claims 26-28 recite that the bus controller sends a bus master selection signal to all of said bus masters along with the grant signal, the selection signal indicating a bus master by which the grant signal is to be received. Such structure completely eliminates stall of the bus use request from the CPU (one of bus masters) until the DMA (the other bus master)'s data transfer is completed, as described, for example, at page 13, lines 29-32 in the specification. Dutton on the other hand fails to disclose this claimed feature, and Claims 27-28 are therefore believed to be further patentably distinguishing over Dutton.

New Claim 29 recites substantially similar features as those stated in Claim 1, and recites that the bus master sends the request signal to the other bus master and the bus controller, and the other bus master determines the availability of each of the unit data buses based on the request signal to send the request signal specifying available unit data bus, whereby utilization of unit data buses is enhanced. Once again, Dutton completely fails to disclose such a claimed feature.

Consequently, in light of the present amendment and for the reasons stated above, Applicants

respectfully submit that the present application is in condition for allowance, and an early and

favorable indication to that effect is respectfully requested.

Respectfully submitted,

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16